**RESTRICTED ACCESS**

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| **DISTRIBUTION :** | **Firm** | **To** | **Ref** | **Copies** | **1st page** | **e-mail** |
|  | FCE | Xavier Christmann, Claude Redon, | 8 |  |  |  |
|  | FCE | Pierre-Olivier Pilot, Sabine Flechelle, Audrey Vaché, M. Pastor, N. Bianchi, A. Dorel, Aki Saito, Sabrine Bouazizi, Wail Amri, Hmaza Zetti | 10 |  |  |  |
|  | RBE | S. Papadineti | 3 |  |  |  |
|  |  |  |  |  |  |  |
|  | FCE | Secretary ship | 1 |  |  |  |

**SW Architecture Design & Interface Description :**

**PRE sw UNIT**

OBJECT: This document is the description of the design & interfaces for *PRE* SW unit.

SUMMARY: This document provides a high-level view of the *PRE* SW unit. The inputs of this document are provided by the software requirement. It is linked to the DAIMLER\_MMA\_SWarchitectureDesignInterfaceDescription document.

CONCLUSION: Applicable from R01.0 SW release

**THIS DOCUMENT CONTAINS HIDDEN TEXT**

EVOLUTION OF THE DOCUMENT

|  |  |  |  |
| --- | --- | --- | --- |
| **Issue** | **Date** | **Author** | **Motive and nature of the modifications** |
| 1 | 31/08/2016 | C. Redon | First release (extract from the full PP4G architecture document) |
| 2 | 26/09/2016 | C. Redon | Specification of the link between the belt function cycles and the corresponding RTE data (shared between BFS and the decision algorithms). |
| 3 | 02/11:2016 | C. Redon | Coverage of TF-R |
| Start extended description based on mainstream document | | | |
| 1.1.1.2 | 15/07/2019 | A. Vaché | Update traceability to match PP4G extended platform requirements IDs |
| 1.1.1.3 | 08/08/2019 | A. Vaché | Solve some traceability issues highlighted by reqtify |
| Start DAI MMA description based on mainstream document | | | |
| 1.1.4.1 | 06/01/2022 | A. Negrea | First revision |
| 1.1.4.2 | 06/01/2022 | A. Negrea | Duplicate revision |
| 1.1.4.3 | 31/01/2022 | A. Negrea | Add inhibition traceability |

This document contains **16** pages.

Peer Review associated to this document: PRWB

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# Documentation

## Upper Level Relevant Documents

This section presents all the documents needed to write the software architecture design document.

|  |  |  |  |
| --- | --- | --- | --- |
| Nb | **Document** | **Reference** | **Company** |
|  | TF-A: To Manage the power supply | /RevAS/30\_DES\_Requirements/Technical Functions/  DES\_TF\_A\_To\_Manage\_The\_Power\_Supply | RBE/FCE |
|  | TF-B: To Manage the communication | /RevAS/30\_DES\_Requirements/Technical Functions/  DES\_TF\_B\_To\_Manage\_The\_Communication | RBE/FCE |
|  | TF-C: To Secure PP ECU functioning using Pictus MCU | /RevAS/30\_DES\_Requirements/Technical Functions/  DES\_TF\_C\_To\_Secure\_PP\_ECU\_Functioning\_Pictus | RBE/FCE |
|  | TF-D: To Program MCU | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_D\_To\_Program\_MCU | RBE/FCE |
|  | TF-E: To Manage Diagnostic Requests | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_E\_To\_Manage\_Diagnostic\_Requests | RBE/FCE |
|  | TF-F: To Perform Measurements | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_F\_To\_Perform\_Measurements | RBE/FCE |
|  | TF-G: To Drive the Motor | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_G\_To\_Drive\_the\_Motor | RBE/FCE |
|  | TF-H: To Perform Autotests | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_H\_To\_Perform\_Autotests | RBE/FCE |
|  | TF-I: To Manage the Failure | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_I\_To\_Manage\_The\_Failure | RBE/FCE |
|  | TF-J: To Manage NVM - NVP (Non Volatile Parameters) | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_J\_To\_Manage\_NVM | RBE/FCE |
|  | TF-K: To Ensure ECU Protection and Integration | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_K\_To\_Ensure\_ECU\_Protection\_And\_Integration | RBE/FCE |
|  | TF-L: To Ensure ECU Integration in Environment EMC ESD | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_L\_To\_Ensure\_ECU\_Integration\_In\_Environment\_EMC\_ESD | RBE/FCE |
|  | TF-M: To generate time base | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_M\_To\_Generate\_Time\_Base | RBE/FCE |
|  | TF-N: To evaluate belt data | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_N\_To\_Evaluate\_Belt\_Data | RBE/FCE |
|  | TF-O: To schedule the SW | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_O\_To\_Run\_SW | RBE/FCE |
|  | TF-P: To handle network management | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_P\_To Handle\_Network\_Management | RBE/FCE |
|  | TF-Q: To Provide Data For Expertise | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_Q\_To\_Provide\_Data\_For\_Expertise | RBE/FCE |
|  | TF-R: To Decide Belt Function Execution | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_R\_To\_Decide\_Belt\_Function\_Execution | RBE/FCE |
|  | TF-S: To drive the boost | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_S\_To\_Drive\_Boost | RBE/FCE |
|  | TF-X: To generate time base | /RevAS/30\_DES\_Requirements/Technical Functions/DES\_TF\_M\_To\_Generate\_Time\_Base | RBE/FCE |

## Design interface description Documents

This section presents all the documents that are linked to this software architecture design document.

Note: All links are related to S:\drive, to have them functional, please mount the S:\drive on your Audi Tr6 extended platform sandbox.

|  |  |  |  |
| --- | --- | --- | --- |
| Nb | **Document** | **Reference** | **Company** |
|  | EEPROM parameters | SBE\_4G\_NVP\_layout.xls | RBE/FCE |
|  | Design Interface description of AdcIf | N/A | RBE/FCE |
|  | Design Interface Description of Auto Tests Manager | N/A | RBE/FCE |
|  | Design Interface Description of Belt Function Decision | N/A | RBE/FCE |
|  | Design Interface Description of Belt Function Execution | [BFE - Design Interface Description.docx](file:///S:\Architectures\Application\Description\Associated_Documents\BFE%20-%20Design%20Interface%20Description%20.docx) | RBE/FCE |
|  | Design Interface Description of Belt Function Selection | [BFS - Design Interface Description.docx](file:///S:\Architectures\Application\Description\Associated_Documents\BFS%20-%20Design%20Interface%20Description%20.docx) | RBE/FCE |
|  | Design Interface Description of Belt Movement Monitoring | N/A | RBE/FCE |
|  | Design Interface Description of Belt Parking Algorithm | N/A | RBE/FCE |
|  | Design Interface Description of Belt Slack Reduction | N/A | RBE/FCE |
|  | Design Interface Description of Basic Software Manager | N/A | RBE/FCE |
|  | Design Interface Description of Basic Software Manager Interface | N/A | RBE/FCE |
|  | Design Interface Description of Can Tranceiver Interface | N/A | RBE/FCE |
|  | Design Interface Description of Communication Interaction Layer | [CIL - Design Interface Description.docx](file:///S:\Architectures\Application\Description\Associated_Documents\CIL%20-%20Design%20Interface%20Description.docx) | RBE/FCE |
|  | Design Interface Description of Diagnostic Communication Manager Interface | N/A | RBE/FCE |
|  | Design Interface Description of Diagnostic Event Manager Interface | N/A | RBE/FCE |
|  | Design Interface Description of DiagOnCAN services management | [DIA - Design Interface Description.docx](file:///S:\Architectures\Application\Description\Associated_Documents\DIA%20-%20Design%20Interface%20Description.docx) | RBE/FCE |
|  | Design Interface Description of Electronic Control Unit Manager | N/A | RBE/FCE |
|  | Design Interface Description of Electronic Control Unit Manager Interface | N/A | RBE/FCE |
|  | Design Interface Description of End of life | N/A | RBE/FCE |
|  | Design Interface Description of Error Handler | N/A | RBE/FCE |
|  | Design Interface Description of Haptic Warning | N/A | RBE/FCE |
|  | Design Interface Description of Memory Integrity Control | N/A | RBE/FCE |
|  | Design Interface Description of Mode Management | [MMG - Design Interface Description.docx](file:///S:\Architectures\Application\Description\Associated_Documents\MMG%20-%20Design%20Interface%20Description.docx) | RBE/FCE |
|  | Design Interface Description of Network Management Interface | N/A | RBE/FCE |
|  | Design Interface Description of Non-Volatile Memory Interface | N/A | RBE/FCE |
|  | Design Interface Description of Non-Volatile Parameters | [NVP - Design Interface Description.docx](file:///S:\Architectures\Application\Description\Associated_Documents\NVP%20-%20Design%20Interface%20Description.docx) | RBE/FCE |
|  | Design Interface Description of Operating System Interface | N/A | RBE/FCE |
|  | Design Interface Description of Power Abstraction Layer | [PAL - Design Interface Description.docx](file:///S:\Architectures\Application\Description\Associated_Documents\PAL%20-%20Design%20Interface%20Description.docx) | RBE/FCE |
|  | Design Interface Description of Pre-Crash Master | N/A | RBE/FCE |
|  | Design Interface Description of Physical Measures Provider | [PMP - Design Interface Description.docx](file:///S:\Architectures\Application\Description\Associated_Documents\PMP%20-%20Design%20Interface%20Description.docx) | RBE/FCE |
|  | Design Interface Description of Port Interface | N/A | RBE/FCE |
|  | Design Interface Description of Pre Pre-Tensioning | [PRE - Design Interface Description.docx](file:///S:\Architectures\Application\Description\Associated_Documents\PMP%20-%20Design%20Interface%20Description.docx) | RBE/FCE |
|  | Design Interface Description of Production cycle function | N/A | RBE/FCE |
|  | Design Interface Description of Pulse Width Modulation Interface | N/A | RBE/FCE |
|  | Design Interface Description of Reset Cause Management | N/A | RBE/FCE |
|  | Design Interface Description of SBC | N/A | RBE/FCE |
|  | Design Interface Description of System Context Management | N/A | RBE/FCE |
|  | Design Interface Description of Standard Function Recovery (releasing function) | [SFR - Design Interface Description.docx](file:///S:\Architectures\Application\Description\Associated_Documents\SFR%20-%20Design%20Interface%20Description.docx) | RBE/FCE |
|  | Design Interface Description of Serial Peripheral Interface Interface | N/A | RBE/FCE |
|  | Design Interface Description of Startup | N/A | RBE/FCE |
|  | Design Interface Description of System Time Management | N/A | RBE/FCE |
|  | Design Interface Description of Vehicle Dynamics algorithm | N/A | RBE/FCE |

## Freescale Documents

This section presents all the documents that complete this software architecture design document.

|  |  |  |  |
| --- | --- | --- | --- |
| Nb | **Document** | **Reference** | **Company** |
|  | MC9S12ZVC-Family Reference Manual Preliminary  Confidential | MC9S12ZVCRM\_Rev0.06.pdf | Freescale |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

## Tier2 Documents

This section presents all the documents that complete this software architecture design document.

|  |  |  |  |
| --- | --- | --- | --- |
| Nb | **Document** | **Reference** | **Company** |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

## HW Datasheet

This section presents all the documents related to the HW components that complete this software architecture design document.

|  |  |  |  |
| --- | --- | --- | --- |
| Nb | **Document** | **Reference** | **Company** |
|  | BTN8984TA datasheet | BTN8984TA\_TDS\_051 | Infineon |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

## Other Documents

This section presents all the documents that also have been needed to write this software architecture design document.

|  |  |  |  |
| --- | --- | --- | --- |
| Nb | **Document** | **Reference** | **Company** |
|  | Unified Modelling Language | 2.1.1 | OMG |
|  | MCU RFQ | [E2581849](https://plm.autoliv.int/linkto/latest/ProductDescription/E2581849/*) | FCE |
|  |  |  |  |

## Glossary And Definition

This section presents all the definitions and/or abbreviations used in this document.

*List of terms in alphabetical order:*

|  |  |
| --- | --- |
| ***Term*** | ***Meaning*** |
| ADC | Analog Digital Converter |
| AEC | Autoliv Error Code |
| API | Application Programming Interface |
| ASDM | Active Safety Domain Master |
| ASIC | Application Specific Integrated Circuit |
| ASY | Active SafetY |
| BSW | Basic SW modules |
| CAN | Controller Area Network |
| C/S | Chip Select |
| COP | Computer Operating Properly |
| eCPL | Electronic Crash Pole Locking |
| DART | Ditch - Airborne - Rough Terrain |
| DFLASH | Data FLASH |
| ECC | Error Code Correction |
| ECU | Electronic Control Unit |
| EOL | End Of Life |
| EEPROM | Electric Erasable and Programmable Read only Memory |
| HFPP | High Force Pre-Pre-Tensioning belt function |
| HF-PRE | High Force PRE pre-tensioning |
| HR | Hard Releasing |
| I/O | Input/Output |
| IMU | Inartial Measurements Unit |
| ISS | Integrated Safing System |
| LFPP | Low Force Pre-Pre-Tensioning belt function |
| MSA | Motor Start/Stop Automatic |
| MCAL | Micro-Controller Abstraction Layer |
| MCU | Micro-controller Unit |
| NMG | Mode ManaGement |
| NVM | Non Volatile Memory |
| OS | Operating System |
| PCM | Pre-Crash Master |
| PFLASH | Program FLASH |
| PIT | Periodic Interrupt Timer |
| PLL | Phase-locked loop |
| RAM | Random Access Memory |
| RCWM | Rear Collision Warning and Mitigation |
| RML | Left PP ECU |
| RMR | Right PP ECU |
| RMx | Both PP ECU |
| ROM | Read Only Memory |
| RSU | Remote Sensor Unit |
| RTE | Real Time Environment |
| RTOS | Real Time Operating System |
| SFR | Standard Function Recovery |
| SODL | Side Obstacle Detection Left |
| SPI | Serial Peripheral Interface |
| SRS | Supplementary Restraint System |
| TBC | To be confirmed |
| TBD | To be defined |
| TF | Technical Function |
| TFLASH | Test FLASH of the Pictus MCU (“one time programmable” memory) |
| W/D | Watchdog |

# Description

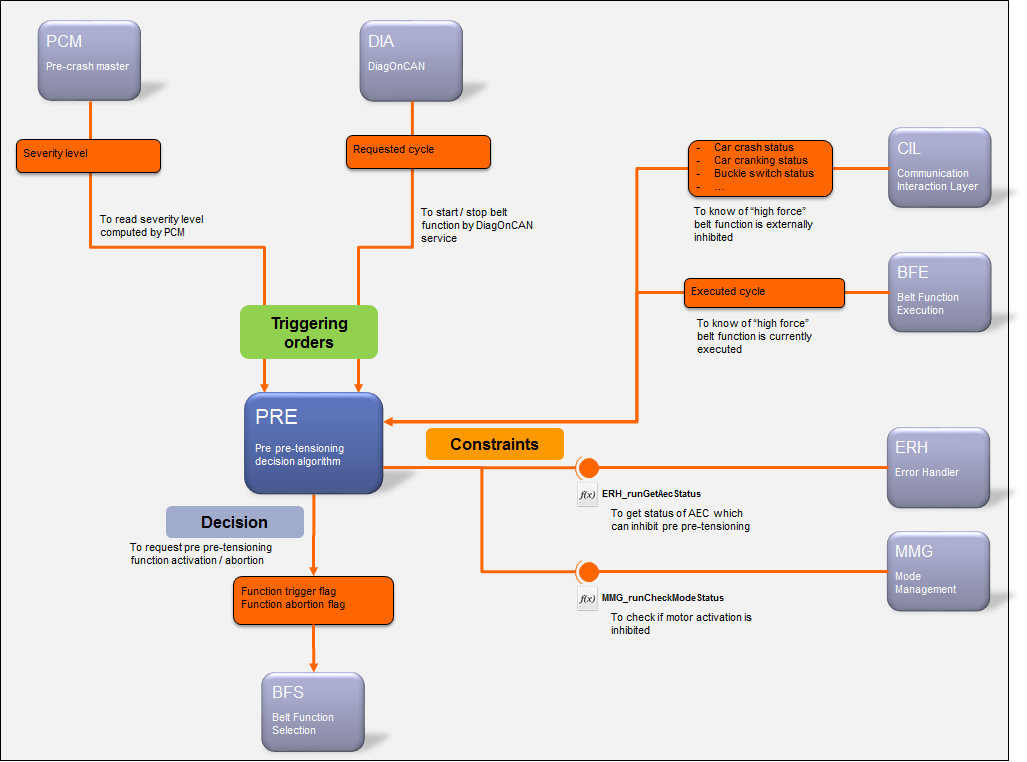
The PRE SW unit is the decision algorithm related to the pre pre-tensioning function.

It is actually an aggregation of sub-components intended to manage different levels of pre-crash severity, each of them leading to request for a particular pre pre-tensioning cycle activation (to BFS).

This component is part of the so called “belt function decision matrix” layer.

As depicted by the figure below, the purpose of the PRE decision algorithm is to request the activation or abortion of the corresponding pre pre-tensioning cycle to BFS in taking into account 2 types of data:

* The **triggering orders** (received from CAN signal and DiagOnCAN service)
* The **constraints** which can inhibit or abort the belt function activation



**Figure 1: Pre - Static description**

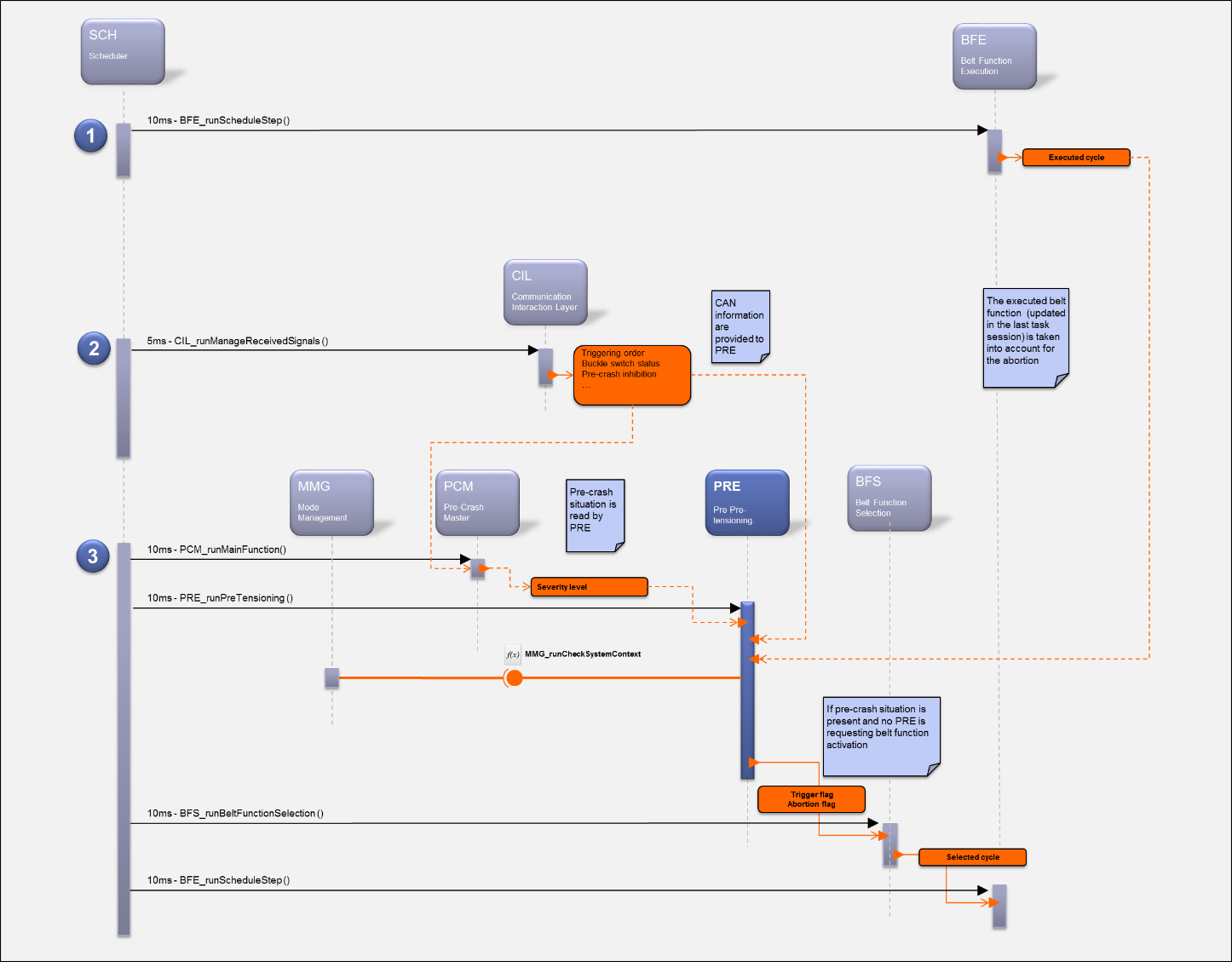
# Technical functions

|  |  |  |  |
| --- | --- | --- | --- |
| **Requirements** | **Criteria** | **Levels/Tolerances** | **Source** |
| ARCH\_SW\_PRE\_0000 | This component shall implement the TF-R6 – TF-R8 technical function. |  |  |

## To start/stop a pre pre-tensioning cycle activation by CAN (nominal case)

The pre pre-tensioning cycle activation sequence is based on information resulting from different sources and real time execution contexts (repeated every 10ms).

1. The first context is related to the belt functions execution from which BFE will provide the current executed cycle.
2. The second context is related to the CAN signals reception from which the CIL component will provide information received form the vehicle (the activation order, buckle switch status…).
3. The last execution context is the one which will call the PRE decision matrixes. At this stage, all information needed by PRE are available to decide if pre pre-tensioning cycle has to be requested, aborted or skipped.



**Figure 2: Pre – To start/stop a pre pre-tensioning cycle activation by CAN**

## To start/stop a pre pre-tensioning cycle activation by DiagOnCAN

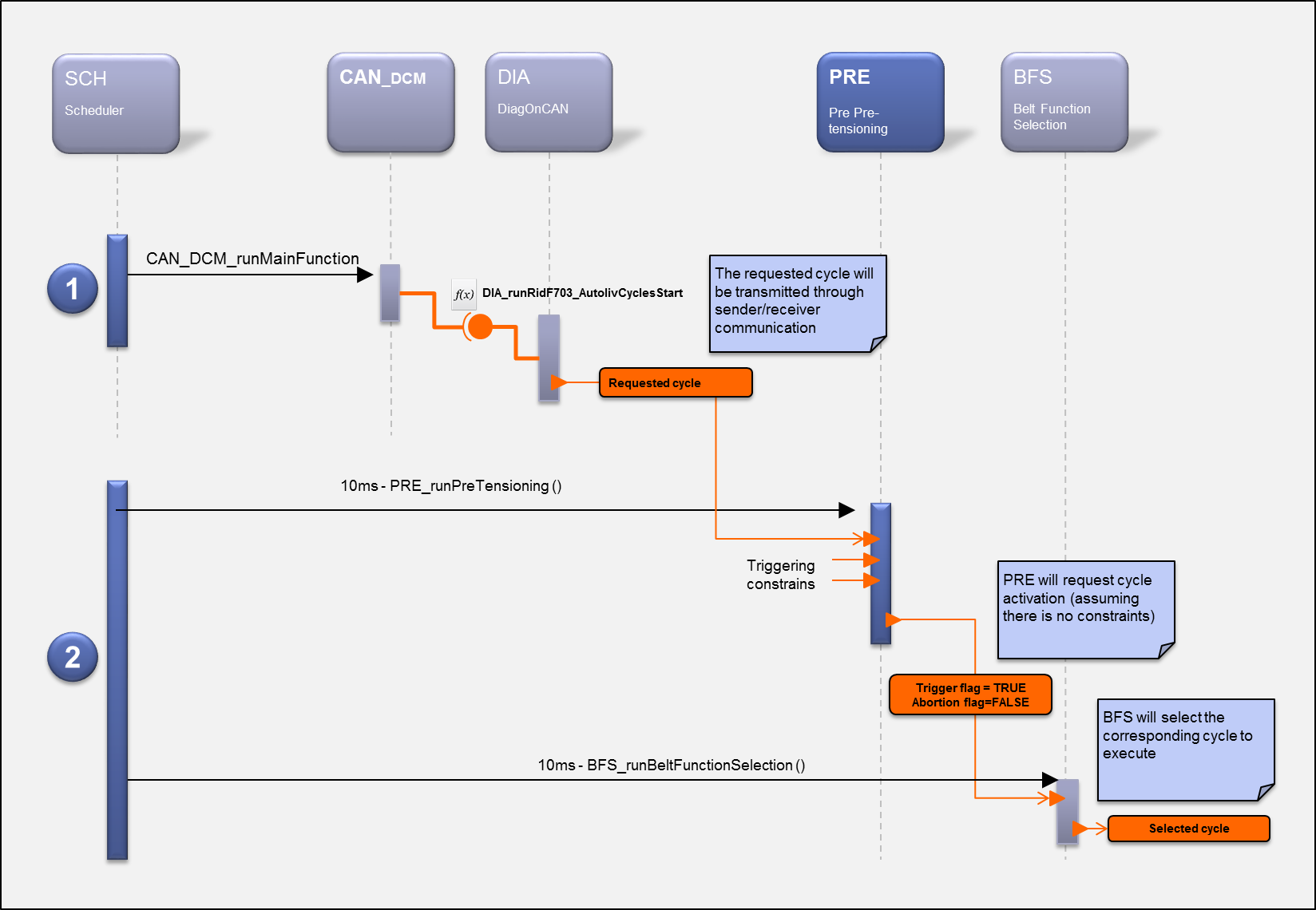
Pre pre-tensioning activation is also possible thank to a dedicated DiagOnCAN service.

As depicted by this figure, the triggering order will be transmitted by DIA to PRE thank to a “sender/receiver” communication.

This will be done in 2 steps:

1. DIA will transmit to PRE the activation order received from the DiagOnCAN triggering service
2. The activation order will be taken into account in the next session of the PRE main function execution

The principle is the same to stop the pre pre-tensioning cycle activation but ordered from another DiagOnCAN service.



**Figure 3: Pre - To start/stop a pre pre-tensioning cycle activation by DiagOnCAN**

# Runnables

## PRE\_runPreTensioning

### Definition

|  |  |  |  |
| --- | --- | --- | --- |
| **Prototype** | | | |
| void **PRE\_runPreTensioning** (void) | | | |
| **Object** | | | |
| This function shall periodically evaluate all the pre pre-tensioning activation orders and constraints in order to request a pre-pre-tensioning cycle triggering or interrupt. | | | |
| **Parameters** | | | |
| Name | Type | Direction | Description |
| NA | NA | NA | NA |
| **Returned value** | | | |
| Name | Description | | |
| NA | NA | | |
| **Dynamic aspect** | | | |
| Periodic – 10ms  Non reentrant | | | |
| **Requirements** | | | |
| ARCH\_SW\_PRE\_0020 | | | |
| **Covered requirements** | | | |
|  | | | |

### Data flow / Parameters

The table below specifies the **input** data related to this runnable. For a complete description of the data flow, refer to [B1].

|  |  |  |  |
| --- | --- | --- | --- |
| **Requirements** | **Criteria** | **Levels/Tolerances** | **Source** |
| ARCH\_SW\_PRE\_0021 | The severity level from CIL shall be an input.  This will be the **primary trigger signal**. |  | DAI\_EXT\_TF\_R\_2380; DAI\_EXT\_TF\_R\_2381; DAI\_EXT\_TF\_R\_2382 |
| ARCH\_SW\_PRE\_0022 | The requested cycle data from DIA shall be an input.  This will be the **secondary** **trigger signal**. |  |  |
| ARCH\_SW\_PRE\_0023 | The PRE\_runPreTensioning function shall take into account the binary complement of the requested cycle data computed by DIA.  This will prevent from inadvertent pre pre-tensioning triggering. |  |  |
| ARCH\_SW\_PRE\_0024 | The buckle switch status from CIL shall be an input. |  |  |
| ARCH\_SW\_PRE\_0025 | The car crash status signal from CIL shall be an input. |  |  |
| ARCH\_SW\_PRE\_0026 | The car cranking status signal from CIL shall be an input. |  |  |
| ARCH\_SW\_PRE\_0027 | The external pre pre-tensioning inhibition status from CIL shall be an input. |  | DAI\_EXT\_TF\_R\_2389 |
| ARCH\_SW\_PRE\_0028 | The internal high force pre pre-tensioning inhibition status from MMG shall be an input. |  | DAI\_EXT\_TF\_R\_2425;  DAI\_EXT\_TF\_R\_2426; DAI\_EXT\_TF\_R\_2433;  DAI\_EXT\_TF\_R\_2434 |
| ARCH\_SW\_PRE\_0029 | The internal low force pre pre-tensioning inhibition status from MMG shall be an input. |  |  |
| ARCH\_SW\_PRE\_0030 | The current executed cycle from BFE shall be an input.  Note:  Since the execution of the belt function is done after the decision, it means that PRE will take into account the executed cycle information updated 10ms earlier in the previous context of the OS task. |  |  |
| ARCH\_SW\_PRE\_0031 | The Factory Mode from NVP shall be an input parameter. |  |  |
| ARCH\_SW\_PRE\_0032 | The Trig OFF status shall be provided by this function. |  |  |

The table below specifies the **output** data related to triggering and interrupt requests. For a complete description of the data flow, refer to [B1].

|  |  |  |  |
| --- | --- | --- | --- |
| **Requirements** | **Criteria** | **Levels/Tolerances** | **Source** |
| ARCH\_SW\_PRE\_0100 | The PRE\_runPreTensioning function shall periodically compute the **trigger** flag PRE #1 to request or not the pre pre-tensioning cycle level #0 **triggering**. |  | ALV\_EXT\_TF\_R\_464 |
| ARCH\_SW\_PRE\_0101 | The PRE\_runPreTensioning function shall periodically compute the **interrupt** flag PRE #1 to request or not the pre pre-tensioning cycle level #0 **interrupt** |  | ALV\_EXT\_TF\_R\_464 |
| ARCH\_SW\_PRE\_0102 | The PRE\_runPreTensioning function shall periodically compute the **trigger** flag PRE #2 to request or not the pre pre-tensioning cycle level #1 **triggering**. |  | ALV\_EXT\_TF\_R\_467 |
| ARCH\_SW\_PRE\_0103 | The PRE\_runPreTensioning function shall periodically compute the **interrupt** flag PRE #2 to request or not the pre pre-tensioning cycle level #1 **interrupt** |  | ALV\_EXT\_TF\_R\_467 |
| ARCH\_SW\_PRE\_0104 | The PRE\_runPreTensioning function shall periodically compute the **trigger** flag PRE #3 to request or not the pre pre-tensioning cycle level #2 **triggering**. |  | ALV\_EXT\_TF\_R\_470 |
| ARCH\_SW\_PRE\_0105 | The PRE\_runPreTensioning function shall periodically compute the **interrupt** flag PRE #3 to request or not the pre pre-tensioning cycle level #2 **interrupt** |  | ALV\_EXT\_TF\_R\_470 |
| ARCH\_SW\_PRE\_0106 | The PRE\_runPreTensioning function shall periodically compute the **trigger** flag PRE #4 to request or not the pre pre-tensioning cycle level #3 **triggering**. |  | ALV\_EXT\_TF\_R\_473 |
| ARCH\_SW\_PRE\_0107 | The PRE\_runPreTensioning function shall periodically compute the **interrupt** flag PRE #4 to request or not the pre pre-tensioning cycle level #3 **interrupt** |  | ALV\_EXT\_TF\_R\_473 |
| ARCH\_SW\_PRE\_0108 | The PRE\_runPreTensioning function shall periodically compute the **trigger** flag PRE #5 to request or not the pre pre-tensioning cycle level #4 **triggering**. |  | ALV\_EXT\_TF\_R\_476 |
| ARCH\_SW\_PRE\_0109 | The PRE\_runPreTensioning function shall periodically compute the **interrupt** flag PRE #5 to request or not the pre pre-tensioning cycle level #4 **interrupt** |  | ALV\_EXT\_TF\_R\_476 |
| ARCH\_SW\_PRE\_0110 | The PRE\_runPreTensioning function shall periodically compute the **trigger** flag PRE #6 to request or not the pre pre-tensioning cycle level #5 **triggering**. |  | ALV\_EXT\_TF\_R\_479 |
| ARCH\_SW\_PRE\_0111 | The PRE\_runPreTensioning function shall periodically compute the **interrupt** flag PRE #6 to request or not the pre pre-tensioning cycle level #5 **interrupt** |  | ALV\_EXT\_TF\_R\_479 |
| ARCH\_SW\_PRE\_0112 | The PRE\_runPreTensioning function shall periodically compute the **trigger** flag PRE #7 to request or not the pre pre-tensioning cycle level #6 **triggering**. |  | ALV\_EXT\_TF\_R\_482 |
| ARCH\_SW\_PRE\_0113 | The PRE\_runPreTensioning function shall periodically compute the **interrupt** flag PRE #7 to request or not the pre pre-tensioning cycle level #6 **interrupt** |  | ALV\_EXT\_TF\_R\_482 |
| ARCH\_SW\_PRE\_0114 | The PRE\_runPreTensioning function shall periodically compute the **trigger** flag PRE #8 to request or not the pre pre-tensioning cycle level #7 **triggering**. |  | ALV\_EXT\_TF\_R\_485, ALV\_EXT\_TF\_R\_487 |
| ARCH\_SW\_PRE\_0115 | The PRE\_runPreTensioning function shall periodically compute the **interrupt** flag PRE #8 to request or not the pre pre-tensioning cycle level #7 **interrupt** | These flags will be linked to the booster function | ALV\_EXT\_TF\_R\_485, ALV\_EXT\_TF\_R\_487 |
| ARCH\_SW\_PRE\_0116 | All the **trigger** flags shall be initialized to FALSE by default. |  | ALV\_EXT\_TF\_R\_465, ALV\_EXT\_TF\_R\_468, ALV\_EXT\_TF\_R\_471, ALV\_EXT\_TF\_R\_474, ALV\_EXT\_TF\_R\_477, ALV\_EXT\_TF\_R\_480, ALV\_EXT\_TF\_R\_483, ALV\_EXT\_TF\_R\_486 |
| ARCH\_SW\_PRE\_0117 | All the **interrupt** flags shall be initialized to B\_FALSE by default. |  | ALV\_EXT\_TF\_R\_465, ALV\_EXT\_TF\_R\_468, ALV\_EXT\_TF\_R\_471, ALV\_EXT\_TF\_R\_474, ALV\_EXT\_TF\_R\_477, ALV\_EXT\_TF\_R\_480, ALV\_EXT\_TF\_R\_483, ALV\_EXT\_TF\_R\_486 |

The table below specifies the **default value** for data related to this runnable. For a complete description of the data flow, refer to [B1].

|  |  |  |  |
| --- | --- | --- | --- |
| **Requirements** | **Criteria** | **Levels/Tolerances** | **Source** |
| ARCH\_SW\_PRE\_1000 | All the inhibition status provided (or not) by PRE shall be initialized to INHIBITED. |  | ALV\_EXT\_TF\_R\_227, ALV\_EXT\_TF\_R\_261, ALV\_EXT\_TF\_R\_291, ALV\_EXT\_TF\_R\_327, ALV\_EXT\_TF\_R\_360, ALV\_EXT\_TF\_R\_391 |
| ARCH\_SW\_PRE\_1001 | All the abortion status provided (or not) by PRE shall be initialized to ABORTED. |  | ALV\_EXT\_TF\_R\_230, ALV\_EXT\_TF\_R\_294, ALV\_EXT\_TF\_R\_330, ALV\_EXT\_TF\_R\_363, ALV\_EXT\_TF\_R\_394 |

# MCU resources

The following requirements on resource consumption objectives apply to the module/package:

|  |  |  |  |
| --- | --- | --- | --- |
| **Requirements** | **Criteria** | **Levels/Tolerances** | **Source** |
| ARCH\_SW\_PRE\_9997 | The ROM size consumed by this component shall not exceed 2K bytes. |  |  |
| ARCH\_SW\_PRE\_9998 | The heap size consumed by this component shall not exceed 200 bytes. |  |  |